WHAT IS CLAIMED IS:

1. A computer system comprising:

a memory;

a first processor which writes writing data into the memory;

a second processor; and

a controller which instructs the second processor to process the writing data based on attribute data representing an attribute of the writing data.

2. The computer system according to claim 1, wherein the attribute data comprises information representing a degree of significance of the writing data.

3. The computer system according to claim 2, wherein the controller instructs the second processor to process the writing data when the attribute data represents a degree of significance which is higher that a predetermined degree of significance.

4. The computer system according to claim 1, wherein the controller comprises an interrupt detector which is incorporated in the second processor and instructs to process the writing data when an interruption is detected.

5. The computer system according to claim 1, wherein the controller comprises a direct memory controller which performs a transfer of the writing data written by the first processor into the memory

to a local memory of the second processor, and after the transfer, notifies the second processor that the transfer is completed.

6. The computer system according to claim 1, wherein the determination unit comprises an address determination unit that determines whether an address on the memory into which the writing data is written by the first processor is in a predetermined area.

7. A computer system comprising:

a memory;

a first processor which writes writing data into the memory;

a second processor;

a register; and

a write detecting unit which detects that the first processor writes the writing data into the memory and stores in the register an address on the memory of the writing data,

wherein the second processor reads the writing data based on the address stored in the register.

8. The computer system according to claim 7, further comprising:

a controller which instructs the second processor to process the writing data when the address is stored in the register.

9. A memory control method for controlling a computer system comprising a memory, a first processor

which writes writing data into the memory, a second processor, and a controller which instructs the second processor to process the writing data, the method comprising:

receiving attribute data representing an attribute of the writing data from the first processor; and

determining whether the controller instructs the second processor to process the writing data based on the attribute data.

10. A memory control method for controlling a computer system comprising a memory, a first processor which writes writing data into the memory, a second processor, a register, and write monitoring means which stores in the register an address on the memory of the writing data,

wherein the second processor reads the writing data based on the address stored in the register.